

CLAIMS

What is claimed is:

- 1 1. A method for controlling the performance of self testing and extended self testing, the
2 method performed by a system that includes a first self test process and a second self test process,
3 the method performed by the system, the method comprising:
4 performing the first self test process in response to a first actuation of a test control by a
5 user of the system;
6 performing the second self test process in response to a second actuation of the test
7 control prior to lapse of a first predefined period of time; and
8 terminating the second self test process in response to a third actuation of the test
9 control by the user of the system, wherein the third actuation is maintained for more than a second
10 predetermined period of time.
- 1 2. The method of claim 1 wherein the test control provides a one-bit binary signal having an
2 actuated state and a non-actuated state.
- 1 3. The method of claim 1 further comprising advancing a presentation of test information in
2 response to a fourth actuation of the test control by the user of the system during performance of
3 the second self test process, wherein the fourth actuation is maintained for less than the second
4 predefined period of time.
- 1 4. The method of claim 1 wherein the first self test process performs legacy functions of the
2 system and the second self test process performs extended functions of the system.
- 1 5. A memory comprising indicia of instructions for performing the method of claim 1.
- 1 6. A system that performs self testing and extended self testing, the system comprising:
2 means for performing the first self test process in response to a first actuation of a
3 provided test control by a user of the system;
4 means for performing the second self test process in response to a second actuation of
5 the test control prior to lapse of a first predefined period of time; and

6 means for terminating the second self test process in response to a third actuation of the
7 test control by the user of the system, wherein the third actuation is maintained for more than a
8 second predetermined period of time.

1 7. The system of claim 6 wherein the test control provides a one-bit binary signal having an
2 actuated state and a non-actuated state.

1 8. The system of claim 6 further comprising means for advancing a presentation of test
2 information in response to a fourth actuation of the test control by the user of the system during
3 performance of the second self test process, wherein the fourth actuation is maintained for less than
4 the second predefined period of time.

1 9. The system of claim 6 wherein the first self test process performs legacy functions of the
2 system and the second self test process performs extended functions of the system.

1 10. A system comprising:

2 a first processor that performs a first self test process in response to a first actuation of a
3 provided test control by a user of the system; and

4 a second processor that performs the second self test process in response to a second
5 actuation of the test control prior to lapse of a first predefined period of time and terminates the
6 second self test process in response to a third actuation of the test control by the user of the system,
7 wherein the third actuation is maintained for more than a second predetermined period of time.

1 11. The system of claim 10 wherein the test control provides a one-bit binary signal having an
2 actuated state and a non-actuated state.

1 12. The system of claim 10 further comprising means for advancing a presentation of test
2 information in response to a fourth actuation of the test control by the user of the system during
3 performance of the second self test process, wherein the fourth actuation is maintained for less than
4 the second predefined period of time.

1 13. The system of claim 10 wherein the first processor further performs legacy functions of the
2 system.

1 14. The system of claim 10 wherein the first processor performs a traffic collision avoidance
2 function and the second processor performs a terrain collision avoidance function.